Development of Cu Damascene Electroplating Machines for Interconnects on Highly Resistive Substrates

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A next-generation interconnect technique for Cu damascene electroplating machines has been developed. This leading-edge technique, which features Cu plating on thin Ru seeds, reduces the terminal effect and enhances uniformity by the placement of a highly resistive element between anodes and cathodes. This technique allows favorable film thickness distribution and film quality, and filling performance.

Keywords: Terminal effect, Cu electroplating, High resistive substrate, Porous resistive element, Ru seed, Uniformity, Filling performance, Surface roughness, Resistivity

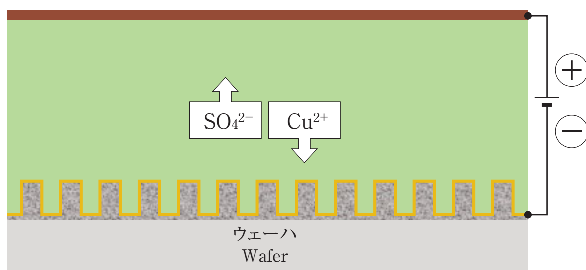


図1　電気めっき処理
Fig. 1　Electroplating on wafer

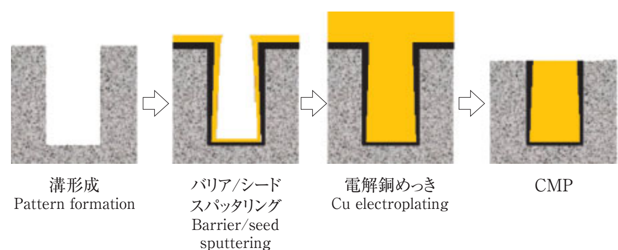


図2　ダマシンプロセス
Fig. 2　Cu damasceme process

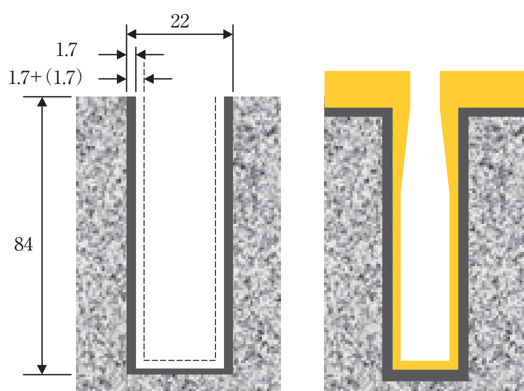


図3　微細化による課題
Fig. 3　Issue of narrower interconnects

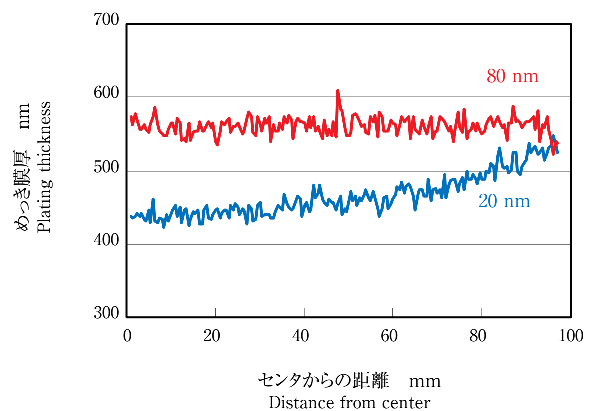


図4　Cu シード薄膜化の課題
Fig. 4　Issue of thinner Cu seed layer

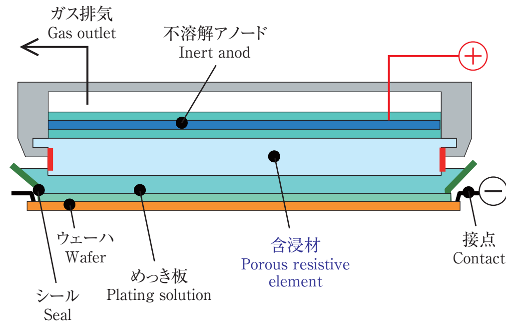


図5　含浸めっきセル
Fig. 5　Plating cell with porous resistive element

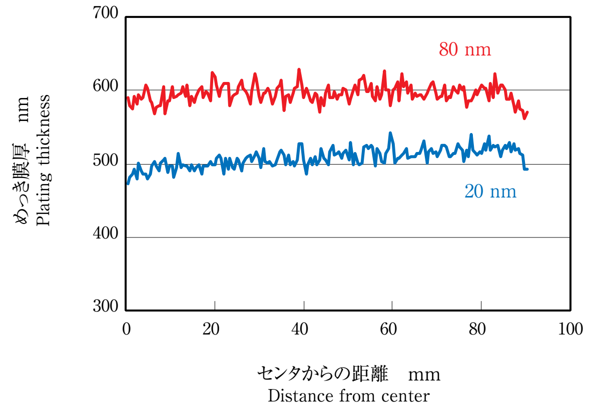


図8　Cu シード薄膜化に対する含浸材の効果
Fig. 8　Effect of porous resistive element on thinner Cu seed layer

図6　含浸材
Fig. 6　Porous resistive element

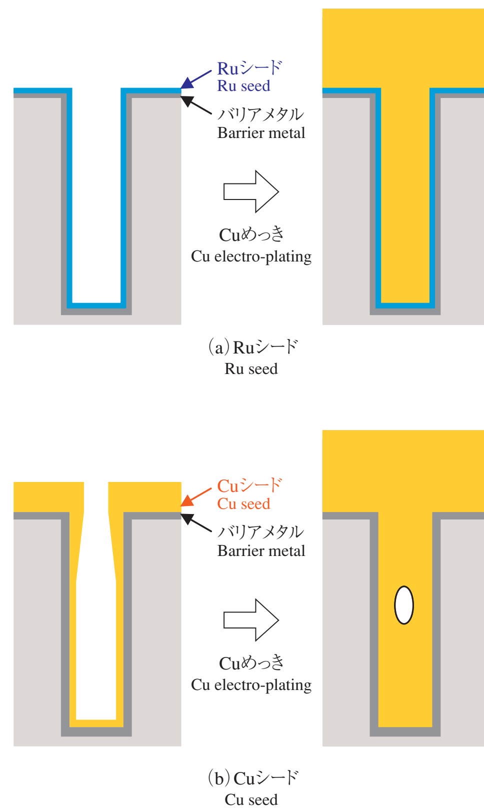


図9　Ru シードと Cu シードの比較
Fig. 9　Comparison between Ru and Cu seed layers

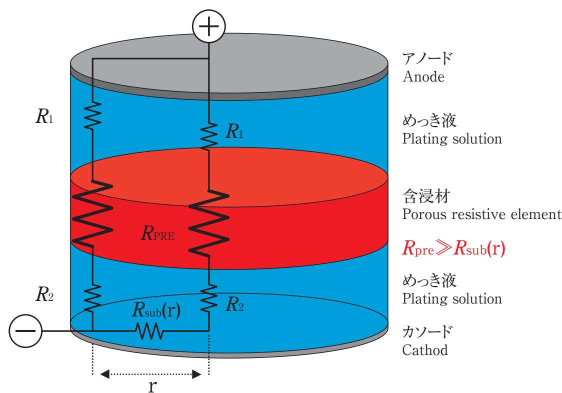


図7　ターミナルエフェクトの緩和
Fig. 7　Terminal-effect reduction

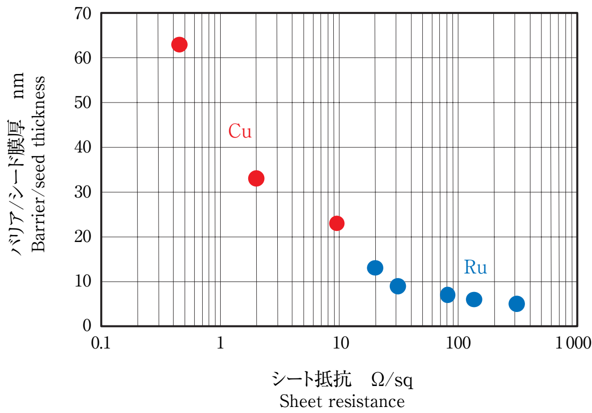


図10　シート抵抗とバリア/シード膜厚の関係
Fig. 10　Relation between sheet resistance and barrier/seed layer

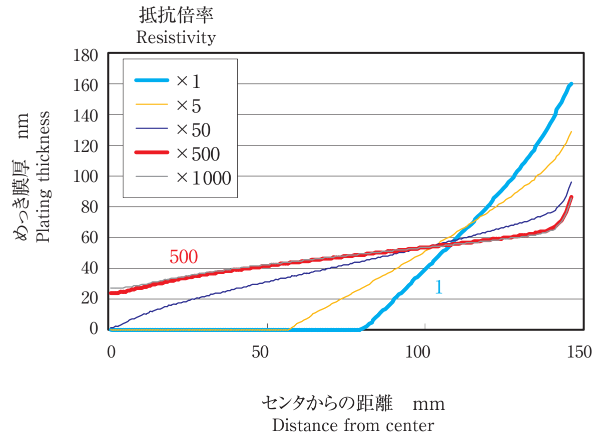
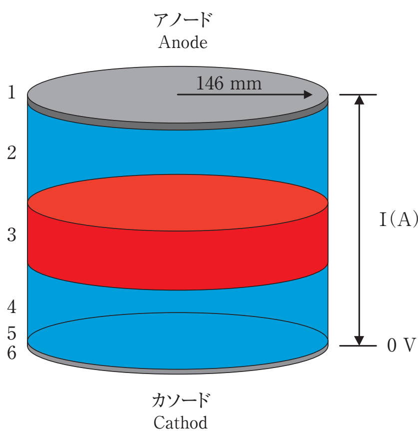


図12　計算結果
Fig. 12　Calculation result



1. アノード分極特性
 Anode polarization
2. めっき液電気伝導度
 Plating-solution conductivity
3. 高抵抗体電気伝導度：めっき液電気伝導度/含浸材抵抗率
 Porous resisitive element conductivity :
 Plating-solution conductivity/Porous resisitive element resisitivity
4. めっき液電気伝導度
 Plating-solution conductivity
5. カソード分極特性
 Cathode polarization
6. 基板電気伝導度
 Substrate conductivity

図11　計算モデル
Fig. 11　Calculation model

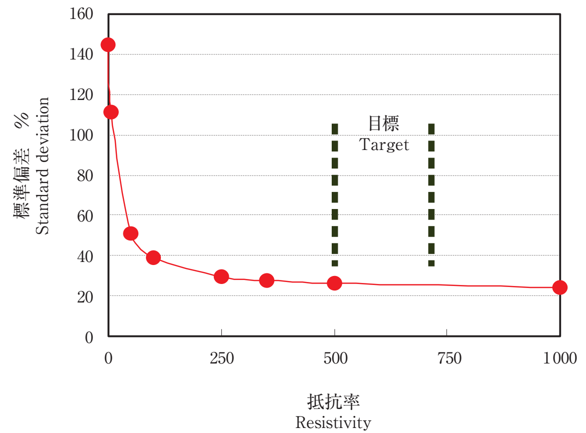


図13　標準偏差の変化
Fig. 13　Changes in standards deviation

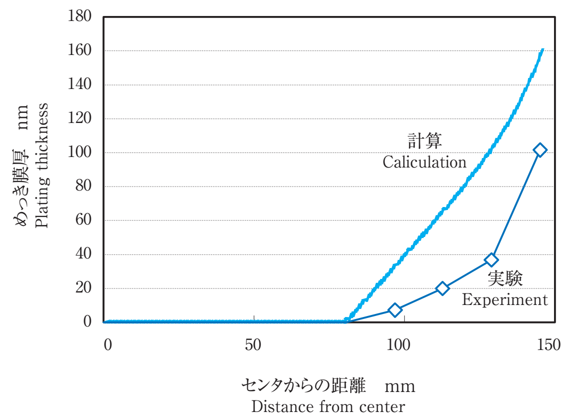
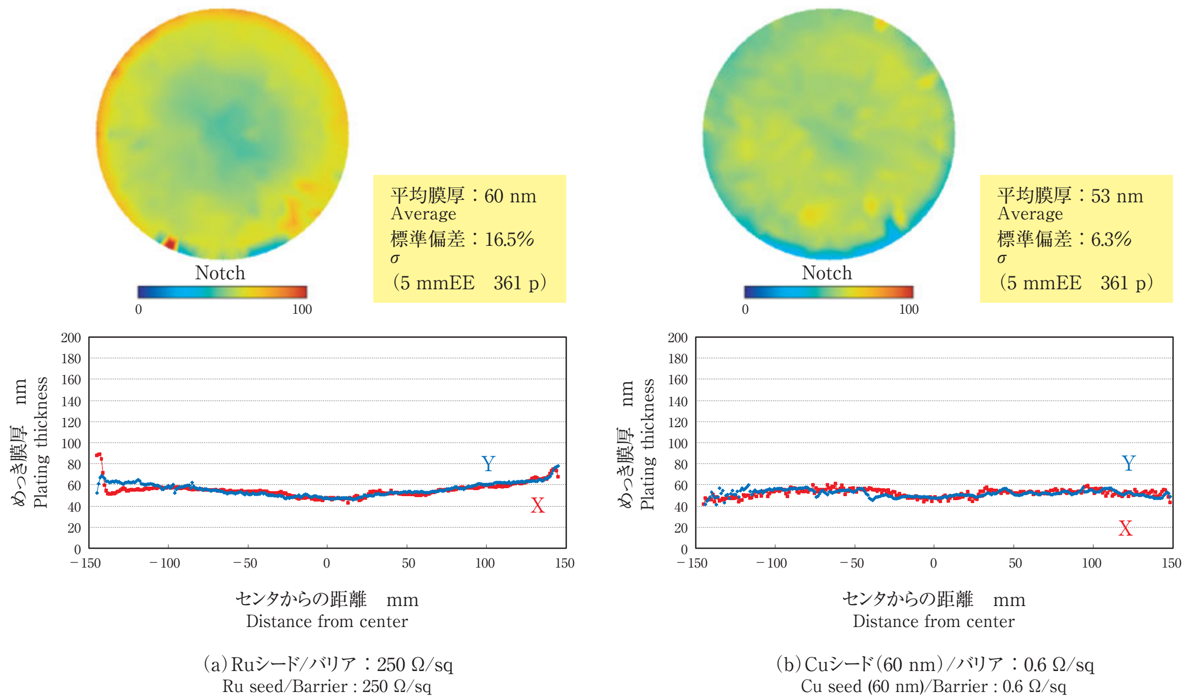


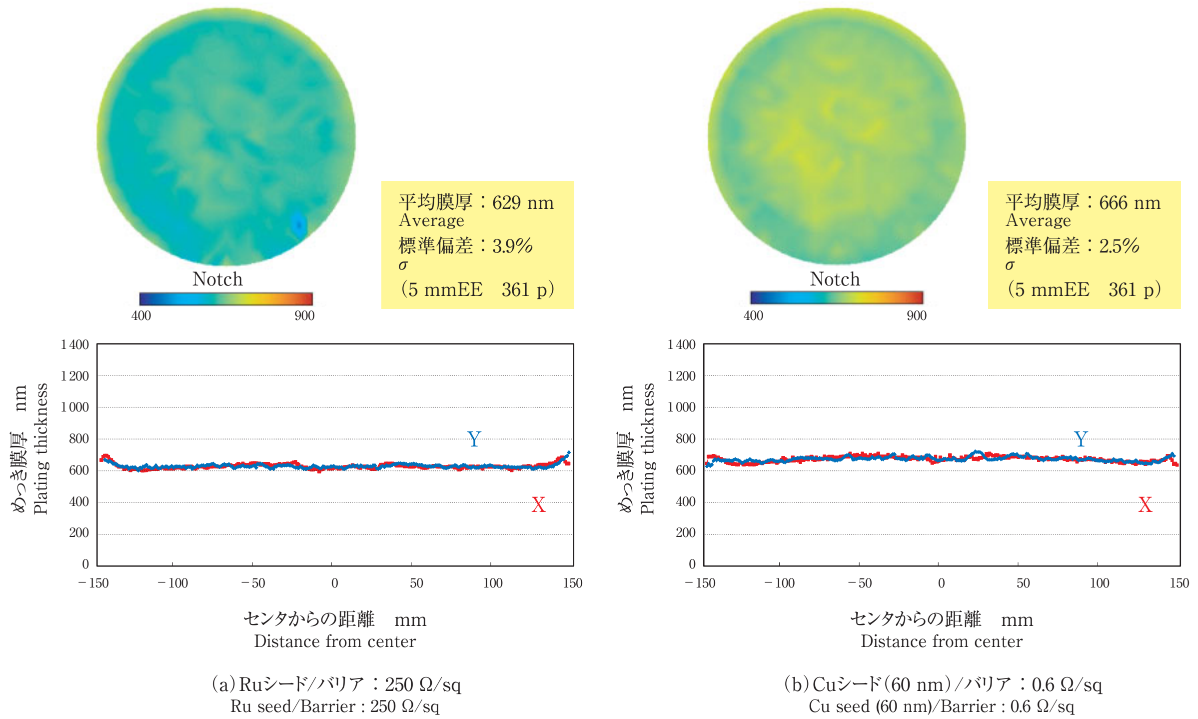
図14　実験と計算結果の比較（抵抗率：1）
Fig. 14　Comparison between experiment and caliculation (Resistivity : 1)



（a）Ruシード/バリア：250 Ω/sq
Ru seed/Barrier : 250 Ω/sq

（b）Cuシード（60 nm）/バリア：0.6 Ω/sq
Cu seed (60 nm)/Barrier : 0.6 Ω/sq

図15　異なるシート抵抗基板上でのめっき均一性比較（1）　抵抗率：700　めっき膜厚：50 nm
Fig. 15　Plating uniformities on substrates of different sheet resistances (1)　Resisitivity : 700　Plating thickness : 50 nm



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（b）Cuシード（60 nm）/バリア：0.6 Ω/sq
Cu seed (60 nm)/Barrier : 0.6 Ω/sq

図16　異なるシート抵抗基板上でのめっき均一性比較（2）　抵抗率：700　めっき膜厚：650 nm
Fig. 16　Plating uniformities on substrates of different sheet resistances (2)　Resisitivity : 700　Plating thickness : 650 nm

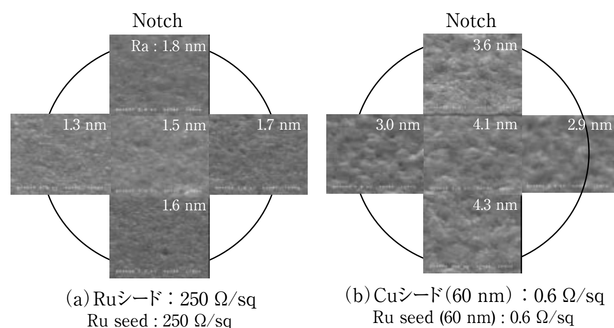

図17　異なるシート抵抗基板上でのめっき表面状態と粗さ比較（1）
抵抗率：700　めっき膜厚：50 nm

Fig. 17　Plating morphologic features and roughneses on substrates of different sheet resistances (1)
Resisitivity : 700　Plating thickness : 50nm

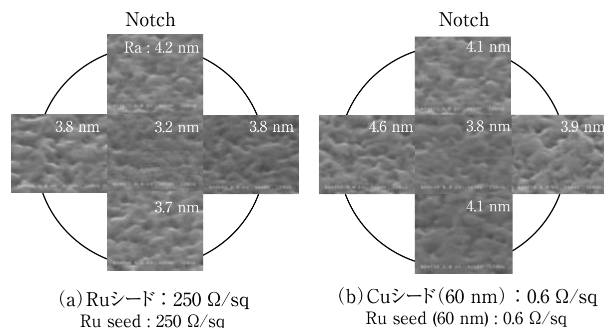

図18　異なるシート抵抗基板上でのめっき表面状態と粗さ比較（2）
抵抗率：700　めっき膜厚：650 nm

Fig. 18　Plating morphologic features and roughneses on substrates of different sheet resistances (2)
Resisitivity : 700　Plating thickness : 650 nm

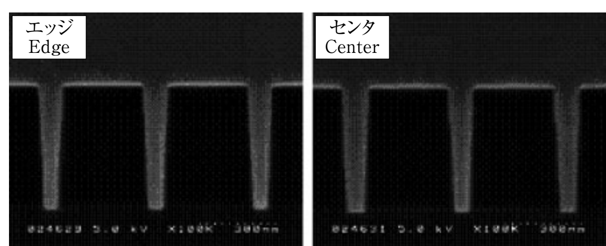

図19　埋設性の評価結果（Cu シード膜）
Fig. 19　Filling resullts (Cu seed layer)